## ABSTRACT OF THE DISCLOSURE

An image display device in which a positive clock signal and a negative clock signal of high frequency are made slightly different in a pulse rise time (tr) and a pulse fall time (tf) from each other to reduce the magnitude of noises each having a sharp waveform which noises are generated in a drive circuit (in particular, a shift register circuit) by being superimposed on each other, thereby providing the image display which has the high picture quality and the high definition and which is free from the turbulence of the image. Delay means is provided in a signal producing unit, a control unit, or an input wiring distributed to the associated circuit in order to shift the phases of the positive clock signal and the negative clock signal from each other by the pulse fall time period (tf), thereby reducing the influence exerted on the display.